Course Information Sheet

Programme:UG	**Degree:** B. Tech (ECE)	
Course Code:	**Course Title: COMPUTER ARCHITECTUR & ORGNIZATION**	
Year: III **Sem:** I **A.Y. :2024-25**	**Regulation:** R20 **University:** JNTU Kakinada.	
L T/P/D C: 3/0/0/3	**Credits: 3**	**Contact Hrs: 4**
Mid Marks: 30	**External Marks: 70**	**Total Marks:** 100
Teaching Hrs: 65	**Exam Duration:** 3 hrs.	
Name of the Faculty	**K. RAGHU**	
Department	**E.C.E**	

Syllabus / Lesson Plan:

COURSE DELIVERY PLAN (LESSON PLAN): Section-A

UNIT-I :

S.No.	Topics to be covered	No. of Classes Required	Teaching Learning Methods	TB and Page Number
1.	Introduction to Basic Structure Of Computers	1	TLM1	T1,24
2.	Functional unit, Basic Operational concepts	1	TLM1	T1,28
3.	Bus structures, System Software	1	TLM1	T1,32
4.	Performance, The history of computer development	1	TLM1	T1,37
5.	Machine Instruction and Programs	1	TLM1	T1,40
6.	Instruction and Instruction Sequencing	1	TLM1	T1,63
7.	Register Transfer Notation	1	TLM1	T1,67
8.	Assembly Language Notation	1	TLM1	T1,71
9.	Basic Instruction Types	1	TLM1	T1,74
No. of classes required to complete UNIT-I		**14**		

UNIT-II :

S.No.	Topics to be covered	No. of Classes Required	Teaching Learning Methods	TB and Page Number
8.	Addressing Modes	2	TLM1	T1,76
9.	Basic Input/output Operations	1	TLM1	T1,79
10.	The role of Stacks and Queues in computer programming equation	2	TLM1	T1,83
11.	Component of Instructions	1	TLM1	T1,88
12.	Logic Instructions, shift and Rotate Instructions	2	TLM1	T1,93
13.	Type of Instructions, Arithmetic and Logic Instructions	2	TLM1	T1,97 T1,101
14.	Branch Instructions	1	TLM1	T1,106
15.	Branch Instructions Addressing Modes, Input/output Operations	1	TLM1	T1,108
No. of classes required to complete UNIT-II		**11**		

UNIT-III :

S.No.	Topics to be covered	No. of Classes Required	Teaching Learning Methods	TB and Page Number
16.	INPUT/OUTPUT ORGANIZATION, Accessing I/O Devices	2	TLM2	T2,99
17.	Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts	2	TLM2	T2,104 T2,107
18.	Handling Multiple Devices, Direct Memory Access	2	TLM2	T2,110 T2,113
19.	Synchronous Bus, Asynchronous Bus	2	TLM2	T2,115
20.	Interface Circuits, Standard I/O Interface	2	TLM2	T2,121 T2,127
21.	Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)	2	TLM2	T2,130
No. of classes required to complete UNIT -III		**12**		

UNIT-IV :

S.No.	Topics to be covered	No. of Classes Required	Teaching Learning Methods	TB and Page Number
24.	The MEMORY SYSTEMS: Basic memory circuits	2	TLM1	T1,202 T1,206
25.	Memory System Consideration, Read- Only Memory: ROM	2	TLM1	T1,210 T1,214
26.	PROM, EPROM, EEPROM	2	TLM1	T1,220
27.	Flash Memory, Cache Memories	1	TLM1	T1,225 T1,227
28.	Mapping Functions, INTERLEAVING	2	TLM1	T1,230 T1,234
29.	**Secondary Storage:** Magnetic Hard Disks,	2	TLM1	T1,237
30.	Optical Disks,	1	TLM1	T1,239
No. of classes required to complete UNIT-IV		**12**		

UNIT-V :

S.No.	Topics to be covered	No. of Classes Required	Teaching Learning Methods	TB and Page Number
31.	Fundamental Concepts: Register Transfers	2	TLM1	T1,332
32.	Performing an Arithmetic Or Logic Operation	2	TLM1	T1,337
33.	Fetching A Word From Memory	2	TLM1	T1,341 T1,343
34.	Execution of Complete Instruction, Hardwired Control,	2	TLM1	T1,349
35.	Micro programmed Control: Microinstructions	2	TLM1	T1,352
36.	Micro program Sequencing	2	TLM1	T1,356
37.	Wide Branch Addressing Microinstructions with next –Address Field	2	TLM1	
No. of classes required to complete UNIT-V		14		
TOTAL		**63**		

Teaching Learning Methods					
TLM1	Chalk and Talk	TLM4	Problem Solving	TLM7	Seminars or GD
TLM2	PPT	TLM5	Programming	TLM8	Lab Demo
TLM3	Tutorial	TLM6	Assignment or Quiz	TLM9	Case Study

Note: Bloom's Taxonomy Levels

BTL1-Remember	**BTL2 – Understand**	**BTL3 –Apply**
BTL4-Analyze	**BT56 –Evaluate**	**BTL6–Create**

Text books (T) / Reference books (R)/Additional text books (A):

T/R/A	Book Title/Author/Publication
T1	Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI
T2	Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition PHI/Pearson, 2012.
A1	Fundamentals or Computer Organization and Design, - Sivaraama Dandamudi Springer Int. Edition, 2003.
A2	J .P. Hayes, "Computer Architecture and Organization",McGraw-Hill,1998

Web References:

W	Web References
W1	https://mrcet.com/downloads/digitalnotes/CSE/III%20Year/COMPUTER%20ORAGANIZATION%20NOTES.pdf
W2	https://nptel.ac.in/courses/106105163/
W3	https://nptel.ac.in/courses/106105165/
W4	https://nptel.ac.in/courses/106105167/
W5	https://nptel.ac.in/courses/106105169/
W6	https://nptel.ac.in/courses/106105159/

CO PO MAPPING:

Computer Organization and Architecture (R2031044)	CO1	Understand and describe the basic organization and operation of the components of a digital computer system.	K1, K2
	CO2	They can analyze the Performance of a computer using performance equation	K3
	CO3	Understanding of different instruction types.	K4
	CO4	Students can calculate the effective address of an operand by addressing modes	K3, K4
	CO5	They can understand how computer stores positive and negative numbers	K2, K5
	CO6	Understand the concepts of I/O Organization and Memory systems.	

CO \ PO Mapping	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	3	3	2	1	2	1	1	1	1		1	1	3	3

CO2	3	3	3	1	3	1			1		1	1	3	3
CO3	2	2	2	1	3	1			1		1	1	3	3
CO4	2	2	2	1	1	1			1		1	1	3	3
CO5	2	2	2	1	1	1			1		1	1	3	3

ASSESSMENT METHODOLOGIES-DIRECT

☑ASSIGNMENTS	☑ STUD. SEMINARS	☑TESTS/MODEL EXAMS	☑UNIV. EXAMINATION
☐ STUD. LAB PRACTICES	☐ STUD. VIVA	☐ MINI/MAJOR PROJECTS	☐ CERTIFICATIONS
☐ ADD-ON COURSES	☐ OTHERS		

ASSESSMENT METHODOLOGIES-INDIRECT

☑ ASSESSMENT OF COURSE OUTCOMES (BY FEEDBACK, ONCE)	☑ STUDENT FEEDBACK ON FACULTY (TWICE)
☐ ASSESSMENT OF MINI/MAJOR PROJECTS BY EXT. EXPERTS	☐ OTHERS

Prepared by **Approved by**