Course Information Sheet

Programme:UG	**Degree:** B.Tech (ECE)	
Course Code:	**Course Title: Switching Theory and Logic Design**	
Year: II **Sem: I** **A.Y. :2024-25**	**Regulation:** **University:** JNTU Kakinada.	
L T/P/D C: 3/0/0/3	**Credits: 3**	**Contact Hrs: 4**
Mid Marks: 30	**External Marks: 70**	**Total Marks:** 100
Teaching Hrs: 60	**Exam Duration:** 3 hrs.	

Course Pre-Requisites: Basic digital electronics.

Course Code	Course Name	Description	Year-Sem
C212	**Switching Theory and Logic Design**	After going through this course the student will be able to 1. Solve a typical number base conversion and analyze new error coding techniques. 2. Understands Theorems and functions of Boolean algebra and behavior of logic gates 3. Optimize logic gates for digital circuits using various techniques. 4. Simplify Boolean function using Karnaugh maps and Quine-McCluskey methods 5. Understand concepts of combinational circuits. 6. Develop advanced sequential circuits.	II ECE Semester –I

Course outcomes:

No.	Description	Skill /Bloom's Taxonomy Level
CO1	Students can able to Classify different number systems and apply to generate various codes.	Understands /BT2
CO 2	Students are able to Use the concept of Boolean algebra in minimization of switching functions	Applying /BT3
CO 3	Students can understand Design different types of combinational logic circuits.	Applying/ BT3
CO4	Students are able to Apply knowledge of flip-flops in designing of Registers and counters	Applying /BT3
CO5	Students can understand The operation and design methodology for synchronous sequential circuits and algorithmic state machines.	Understanding/ BT2

Course Articulation Matrix:

Mapping of Course Outcomes (CO) with Program Outcomes (PO) and Program Specific Outcomes (PSO's):

Course Outcomes (CO)	Program Outcomes (PO)												Program Specific Outcomes (PSO's)	
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
C212.1	2	1	--										2	-
C212.2	2	2	--										3	-
C212.3	2	2	1										3	-
C212.4	2	2	2										3	-
C212.5	1	2	2										3	-
Overall	**1.8**	**1.8**	**1**										**2.8**	**-**

Level: 1- Low correlation (Low), 2- Medium correlation (Medium), 3-High correlation (High)

JUSTIFICATIONS OF CO –PO MAPPING

C212.1		
C212.1-PO1	2	Students can able to Demonstrate a clear understanding of Number systems conversions and error correction.
C212.1-PO2	1	Able to use different simplification methods to reduce Boolean functions.
C212.1-PO3	--	
C212.1-PO4	--	
C212.1-PO5	--	
C212.1-PO6	--	
C212.1-PO7	--	
C212.1-PO8	--	
C212.1-PO9	--	
C212.1-PO10	--	
C212.1-PO11	--	
C212.1-PO12	--	

C212.2		
C212.2-PO1	2	Students will understands different methods to simplify the given Boolean functions.
C212.2-PO2	2	Students are able to Design simple combinational circuits.
C212.2-PO3	--	
C212.2-PO4		
C212.2-PO5		
C212.2-PO6	--	
C212.2-PO7	--	
C212.2-PO8	-	
C212.2-PO9	--	
C212.2-PO10	--	
C212.2-PO11	-	
C212.2-PO12	--	

C212.3		
C212.3-PO1	2	Understand the behaviour of different combinational circuits.
C212.3-PO2	2	Students will Analyse the behaviour of combinational circuits.
C212.3-PO3	1	Able to analyze the characteristics of the combinational circuits.
C212.3-PO4		
C212.3-PO5		
C212.3-PO6	--	
C212.3-PO7	--	
C212.3-PO8	--	
C212.3-PO9	--	
C212.3-PO10	--	
C212.3-PO11	--	
C212.3-PO12	--	

C212.4		
C212.4-PO1	2	Students are able to Know various Programmable Logic circuits.
C212.4-PO2	2	Students will be able to analyse different Programmable Logic circuits.
C212.4-PO3	2	Students will be able to design different Programmable Logic circuits.
C212.4-PO4		
C212.4-PO5	--	
C212.4-PO6	--	
C212.4-PO7	--	
C212.4-PO8	--	
C212.4-PO9	--	
C212.4-PO10	--	
C212.4-PO11	--	
C212.4-PO12	--	

C212.5

C212.5-PO1	1	Able to understand various synchronous sequential circuits.
C212.5-PO2	2	Students can analyse various applications using synchronous sequential circuits.
C212.5-PO3	2	
C212.5-PO4	--	
C212.5-PO5		
C212.5-PO6	--	
C212.5-PO7	-	
C212.5-PO8	-	
C212.5-PO9	--	
C212.5-PO10	--	
C212.5-PO11	--	
C212.5-PO12	--	

Justification for Avg CO-PO Mapping		
Mapping	**Level**	**Justification**
C212.PO1	1.8	Number system conversions are used in designing engineering systems for solving engineering problems
C212.PO2	1.8	Different simplifications methods used in designing engineering systems to analyze complex engineering problems
C212.PO3	1	Different combinational circuits used in designing engineering systems for solving engineering problems related to public health and safety and environmental systems
C212.PO4		
C212.PO5		
C212.PO6	--	
C212.PO7	--	
C212.PO8	--	
C212.PO9	--	
C212.PO10	--	
C212.PO11	--	
C212.PO12	--	

Justification for CO-PSO Mapping

Mapping	Level	Justification
C212.1-PSO1	2	Students get a sound knowledge of of choosing different conversion methods and error correction methods used in designing
C212.2-PSO1	3	Students learn the Boolean reduction techniques required for designing
C212.3-PSO1	3	Knowledge of combinational circuit design which is used in automation industry
C212.4-PSO1	3	Students understand few of the modules required to design a sequential circuits.
C212.5-PSO1	3	Only overview synchronous sequential circuits.
C212.1-PSO2	--	
C212.2-PSO2	--	
C212.3-PSO2	--	
C212.4-PSO2		
C212.5-PSO2		

Topics beyond Syllabus

S.No.	Description	Proposed Actions
1	Digital circuits design using CMOS	Seminar

TOPICS BEYOND SYLLABUS/ASSIGNMENT/INDUSTRY VISIT/PROJECTS/NPTEL ETC

Topic beyond Syllabus: Mapping with PO and PSO:

Topic beyond syllabus	Program Outcomes (PO)												Program Specific Outcomes (PSO's)	
1.	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
	3	3	2	-	-	-	-	-	-	-	-	-	3	2

Justification for Topic beyond the Syllabus (TBS) -PO Mapping.

Mapping	Level	Justification
TBS-PO1	3	Students could apply the acquired knowledge of digital circuit analysis
TBS-PO2	3	Able to analyze applications of digital circuit analysis
TBS-PO3	2	Able to design various systems using digital circuits.

Justification for Topic Beyond the Syllabus (TBS) -PSO Mapping.

Mapping	Level	Justification
TBS-PSO1	3	Apply the acquired knowledge of design and development of digital circuit design.
TBS-PSO2	2	Analyze the Conventional Methods for various applications to design digital circuits.

WEB SOURCE REFERENCES :

1	**https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/**
2	https://www.geeksforgeeks.org/cmos-logic-gate/

Syllabus / Lesson Plan:

S.No.	SYLLABUS	Periods	Methodology	Text book/references /web references and additional text book reference
	UNIT – I			
1	REVIEW OF NUMBER SYSTEMS & CODES: Representation of numbers of different radix	2	**Chalk & Talk**	**T1, T2, R3**
2	Conversation from one radix to another radix	2	**Chalk & Talk,**	**T1, T2, R3**
3	r-1's compliments and r's compliments of signed members	1	**Chalk & Talk,**	**T1, T2, R3**
4	Gray code ,4 bit codes; BCD, Excess-3, 2421, 84-2-1 code etc	1	**Chalk & Talk,**	**T1, T2, R3**
5	Error detection & correction codes: parity checking, even parity, odd parity	1	**Chalk & Talk**	**T1, T2, R3**
6	Hamming code.	1	**Chalk & Talk**	**T1, T2, R3**
7	BOOLEAN THEOREMS AND LOGIC OPERATIONS: Boolean theorems, principle of complementation	2	**Chalk &Talk**	**T1, T2, R3**

	& duality, De-morgan theorems.			
8	Logic operations ; Basic logic operations -NOT, OR, AND, Universal Logic operations, EX-OR, EX- NOR operations.	1	**Chalk & Talk**	**T1, T2, R3**
9	Standard SOP and POS Forms	1	**Chalk & Talk**	**T1, T2, R3**
10	NAND-NAND and NOR-NOR realizations,	1	**Chalk & Talk**	**T1, T2, R3**
	Total	**13**		
	Unit 2			
11	MINIMIZATION TECHNIQUES: Minimization and realization of switching functions using Boolean theorems.	2	**Chalk & Talk**	**T1, T2, R3**
12	K-Map (up to 6 variables)	2	**Chalk & Talk**	**T1, T2, R3**
13	Tabular method(Quine-mccluskey method) with only four variables and single function.	1	**Chalk & Talk**	**T1, T2, R3**
14	COMBINATIONAL LOGIC CIRCUITS DESIGN: Design of Half adder, full adder	1	**Chalk & Talk**	**T1, T2, R3**
15	half subtractor, full subtractor, applications of full adders.	1	**Chalk & Talk**	**T1, T2, R3**
16	4- bit adder-subtractor circuit	1	**Chalk & Talk**	**T1, T2, R3**
17	BCD adder circuit, Excess 3 adder circuit	1	**Chalk & Talk**	**T1, T2, R3**
18	carry look-a- head adder circuit	1	**Chalk & Talk**	**T1, T2, R3**
19	Design code converts using Karnaugh method and draw the complete circuit diagrams.	2	**Chalk & Talk**	**T1, T2, R3**
	Total	**12**		
	Unit 3			
20	COMBINATIONAL LOGIC CIRCUITS DESIGN USING MSI &LSI : Design of encoder, decoder	2	**Chalk & Talk**	**T1, T2, R3**
21	Multiplexer and de-multiplexers,	2	**Chalk & Talk**	**T1, T2, R3**
22	Implementation of higher order circuits using lower order circuits .	1	**Chalk & Talk**	**T1, T2, R3**
23	Realization of Boolean functions using decoders and multiplexers	1	**Chalk & Talk**	**T1, T2, R3**
24	Design of Priority encoder, 4-bit digital comparator and seven segment decoder.	3	**Chalk & Talk**	**T1, T2, R3**
25	INTRODUCTION OF PLD's : PLDs: PROM, PAL, PLA -Basics structures,	1	**Chalk & Talk**	**T1, T2, R3**
26	Realization of Boolean functions, Programming table.	2	**Chalk & Talk**	**T1, T2, R3**
	Total	**12**		
	Unit 4			
27	SEQUENTIAL CIRCUITS I: Classification of sequential circuits (synchronous and asynchronous)	1	**Chalk & Talk**	**T1, T2, R3**

28	operation of NAND & NOR Latches and flip-flops; truth tables and excitation tables of RS flip-flop	1	**Chalk & Talk**	**T1, T2, R3**
29	JK flip- flop, T-flip-flop, D flip-flop with reset and clear terminals.	2	**Chalk & Talk**	**T1, T2, R3**
30	Conversion from one flip-flop to another flip- flop	1	**Chalk & Talk**	**T1, T2, R3**
31	Design of 5 ripple counters	1	**Chalk & Talk**	**T1, T2, R3**
32	Design of synchronous counters	1	**Chalk & Talk**	**T1, T2, R3**
33	Johnson counter, ring counter.	1	**Chalk & Talk**	**T1, T2, R3**
34	Design of registers - Buffer register, control buffer register	1	**Chalk & Talk**	**T1, T2, R3**
35	Shift register, bidirectional shift register, universal shift, register	2	**Chalk & Talk**	**T1, T2, R3**
36	Study the following relevant ICs and their relevant functions 7474,7475,7476,7490,7493,74121	1	**Chalk & Talk**	**T1, T2, R3**
	TOTAL	**12**		
	UNIT - V			
37	SEQUENTIAL CIRCUITS II : Finite state machine	1	**Chalk & Talk**	**T1, T2, R3**
38	state diagrams, state tables,	2	**Chalk & Talk**	**T1, T2, R3**
39	reduction of state tables	1	**Chalk & Talk**	**T1, T2, R3**
40	Analysis of clocked sequential circuits Mealy to Moore conversion and vice-versa	3	**Chalk & Talk**	**T1, T2, R3**
41	Realization of sequence generator	1	**Chalk & Talk**	**T1, T2, R3**
42	Design of Clocked Sequential Circuit to detect the given sequence (with overlapping or without overlapping)	3	**Chalk & Talk**	**T1, T2, R3**
	TOTAL	**11**		
	GRAND TOTAL	**60**		

Topic Beyond Syllabus:

S.No.	Topic Beyond Syllabus Planning	PERIODS	Methodology	Text book/references/web references and additional text book reference
1	Digital circuits design using CMOS	**1**	**Seminar / Assignment**	**https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/**

Note: Bloom's Taxonomy Levels

BTL1-Remember	**BTL2 – Understand**	**BTL3 –Apply**
BTL4-Analyze	**BT56 –Evaluate**	**BTL6–Create**

Text books (T) / Reference books (R)/Additional text books (A):

T/R/A	Book Title/Author/Publication
T1	Switching and finite automata theory Zvi.KOHAVI,Niraj.K.Jha 3rdEdition,Cambridge UniversityPress,2009
T2	Digital Design by M.MorrisMano, Michael D Ciletti,4th editionPHIpublication,2008
T3	Switching theory and logic design by Hill and Peterson,Mc-Graw Hill TMH edition, 2012.
R1	Fundamentals of Logic Design by Charles H. Roth Jr,JaicoPublishers,2006
R2	Digital electronics by R S Sedha.S.Chand &companylimited,2010
R3	Switching Theory and Logic Design by A. AnandKumar,PHI Learningpvtltd,2016.
R4	Digital logic applications and design by John M Yarbough, Cengagelearning,2006.
R5	TTL 74-Seriesdatabook.

Web References:

W	Web References
W1	https://en.wikipedia.org/wiki/Digital_electronics
W2	https://www.electronicsforu.com/technology-trends/learn-electronics/digital-circuit-design-types-applications-examples
W3	https://www.allaboutcircuits.com/textbook/digital/
W4	https://www.elprocus.com/what-is-digital-circuit-design-and-its-applications/
W5	https://www.sciencedirect.com/topics/engineering/digital-circuits
W6	https://www.tutorialspoint.com/digital-electronics/index.htm

ASSESSMENT METHODOLOGIES-DIRECT

☑ASSIGNMENTS	☑ STUD. SEMINARS	☑TESTS/MODEL EXAMS	☑UNIV. EXAMINATION
☐ STUD. LAB PRACTICES	☐ STUD. VIVA	☐ MINI/MAJOR PROJECTS	☐ CERTIFICATIONS
☐ ADD-ON COURSES	☐ OTHERS		

ASSESSMENT METHODOLOGIES-INDIRECT

☑ ASSESSMENT OF COURSE OUTCOMES (BY FEEDBACK, ONCE)	☑ STUDENT FEEDBACK ON FACULTY (TWICE)
☐ ASSESSMENT OF MINI/MAJOR PROJECTS BY EXT. EXPERTS	☐ OTHERS

Prepared by **Approved by**